IN THE CLAIMS:

Please add new Claims 50 to 55 and amend Claims 28 to 31 and 39 as shown below. The claims, as pending in the subject application, read as follows:

1. to 27. (Canceled).

28. (Currently Amended) An information processing apparatus comprising:

processing means; and

mode setting means for setting a mode of a memory,

wherein said processing means sets said mode setting means ~~in~~ to an ~~enable~~ enabled state in which said mode setting means is allowed to set the memory to a power saving mode, and ~~commands the memory to issue therefrom~~ reads a power saving mode transfer instruction from the memory for setting said processing means ~~in~~ to a power saving mode, and

wherein said mode setting means sets the memory ~~in a~~ to the power saving mode while the mode setting means is in the enabled state, and wherein the memory is set to the power saving mode in accordance with ~~a signal~~ information which relates to the setting of said processing means ~~in~~ to the power saving mode ~~and inputted to said mode setting means while said mode setting means is in the enabling state~~.

29. (Currently Amended) An information processing apparatus according to claim 28, further comprising detecting means for detecting an instruction fetch transfer for the power saving mode transfer instruction and outputting the ~~signal~~ information in

accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction, and wherein said mode setting means sets the memory ~~in~~ to the power saving mode in accordance with the ~~signal~~ information inputted from said detecting means while said mode setting means is in the enabling state.

30. (Currently Amended) An information processing apparatus according to claim 28, wherein if said processing means detects an interruption for returning to the normal operation mode from the power saving mode, said processing means returns a normal operation mode from the power saving mode and invalidates the ~~signal~~ information relating to the setting of said processing means ~~in~~ to the power saving mode, and

wherein said mode setting mode sets the memory in a normal operation mode in accordance with invalidation of the ~~signal~~ information relating to the setting of said processing means ~~in~~ to the power saving mode.

31. (Currently Amended) An information processing apparatus according to claim 28, wherein said processing means outputs the ~~signal~~ information for notifying said mode setting means that said processing means is transferred to the power saving mode, and

wherein said mode setting means sets the memory ~~in~~ to the power saving mode in accordance with the ~~signal~~ information inputted from said processing means while said mode setting means is in the enabled state.

32. (Currently Amended) An information processing apparatus according to claim 28, wherein said mode setting means sets the memory ~~in~~ to the power saving mode after an end of memory transfer in progress.

33. (Currently Amended) An information processing apparatus comprising:

processing means; and

mode transfer means for transferring a mode of a memory,

wherein said processing means sets said mode transfer means ~~in~~ to a waiting state, and executes a power saving mode transfer instruction for setting said processing means ~~in~~ to a power saving mode, and

said mode transfer means transfers the memory to a power saving mode after the end of the waiting state.

34. (Previously presented) An information processing apparatus according to claim 33, wherein said mode transfer means supplies the memory with a predetermined signal to transfer the memory to the power saving mode from a normal operation mode.

35. (Previously presented) An information processing apparatus according to claim 33, wherein said mode transfer means transfers the memory to a normal operation mode in accordance with an interruption for returning said processing means to a normal operation mode from the power saving mode.

36. (Previously presented) An information processing apparatus according to claim 33, wherein said processing means sets a time of period of the waiting state, and said mode transfer means transfers the memory to the power saving mode after a lapse of the time of period of the waiting state.

37. (Previously presented) An information processing apparatus according to claim 33, wherein said processing means instructs said mode transfer means to start counting a lapse of a time period of the waiting state.

38. (Previously presented) An information processing apparatus according to claim 33, wherein said mode transfer means transfers the memory to the power saving mode after an end of memory transfer in progress.

39. (Currently Amended) A power saving controlling method for a processor and a memory, the method comprising:

an ~~enable~~ enabled state setting step of setting a memory controller for controlling the memory ~~in~~ to an ~~enable~~ enabled state in which the memory controller is allowed to set the memory to a power saving mode;

a ~~requesting~~ reading step of ~~commanding the memory to issue therefrom~~ reading a power saving mode transfer instruction from the memory for setting the processor ~~in~~ to a power saving mode; and

a power saving mode setting step of setting the memory ~~in~~ to a power saving mode while the memory controller is in the enabled state, and wherein the memory is set to the power saving mode in accordance with ~~a signal~~ information which relates to

the setting of the processor ~~in~~ to the power saving mode ~~and inputted to the memory controller while memory controller is in the enabling state~~.

40. (Currently Amended) A power saving controlling method according to claim 39, further comprising:

a detecting step of detecting an instruction fetch transfer for the power saving mode transfer instruction; and

an outputting step of outputting the ~~signal~~ information in accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction, and

wherein the memory is set ~~in~~ to the power saving mode at said ~~enable~~ enabled state setting step in accordance with the ~~signal~~ information outputted in said detecting step while the memory controller is in the enabling state.

41. (Currently Amended) A power saving controlling method according to claim 39, further comprising:

a returning step of returning the processor to a normal operation mode from the power saving mode in accordance with an interruption;

an invalidating step of invalidating the ~~signal~~ information relating to the setting of the processor in the power saving mode in accordance with the returning to the normal operation mode of the processor; and

a returning step of returning the memory to a normal operation mode in accordance with invalidation of the ~~signal~~ information relating to the setting of the processor ~~in~~ to the power saving mode.

42. (Currently Amended) A power saving controlling method according to claim 38, further comprising an outputting step of outputting the ~~signal~~ information for notifying memory controller that the processor is transferred to the power saving mode, and

wherein the memory is set ~~in~~ to the power saving mode at said power saving mode setting step in accordance with the ~~signal~~ information outputted at said outputting step while said mode setting means is in the enabling state.

43. (Currently Amended) A power saving controlling method according to claim 39, wherein the memory is set ~~in~~ to the power saving mode at said power saving mode setting step after an end of memory transfer in progress.

44. (Currently Amended) A power saving controlling method for a processor and a memory, the method comprising:

a setting step of setting a memory controller for controlling the memory ~~in~~ to a waiting state;

an executing step of executing a power saving mode transfer instruction for setting the processor ~~in~~ to a power saving mode; and

a transferring step of transferring the memory to a power saving mode after the end of the waiting state.

45. (Previously presented) A power saving controlling method according to claim 44, wherein said transferring step supplies the memory with a predetermined signal to transfer the memory to the power saving mode from a normal operation mode.

46. (Previously presented) A power saving controlling method according to claim 44, further comprising a returning step of returning the memory to a normal operation mode in accordance with an interruption for returning the processor to a normal operation mode from the power saving mode.

47. (Previously presented) A power saving controlling method according to claim 44, further comprising a setting step of setting a time of period of the waiting state, and wherein the memory is transferred to the power saving mode in said transferring step after a lapse of the time of period of the waiting state.

48. (Previously presented) A power saving controlling method according to claim 44, further comprising an instructing step of instructing the memory controller to start counting a lapse of a time period of the waiting state.

49. (Previously presented) A power saving controlling method according to claim 44, wherein the memory is transferred to the power saving mode after an end of memory transfer in progress.

50. (New) An information processing apparatus comprising:

processing means;

setting means for setting a mode of a memory; and

detecting means for detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting said processing means to a power

saving mode, wherein said signal is detected on a bus to which said processing means is connected, and

wherein said setting means sets the memory to the power saving mode in a case where said setting means is allowed to set the memory to the power saving mode and where said signal is detected by said detecting means.

51. (New) An information processing apparatus according to claim 50, wherein the signal detected by said detecting means relates to an instruction fetch transfer for fetching the power saving mode transfer instruction from the memory for setting said processing means to the power saving mode.

52. (New) An information processing apparatus according to claim 50, wherein said setting means sets the memory to the power saving mode after an end of memory transfer in progress in a case where said setting means is allowed to set the memory to the power saving mode and where the signal relating to reading the power saving mode transfer instruction from the memory for setting said processing means to the power saving mode is detected by said detecting means.

53. (New) A power saving controlling method for a processor and a memory, the method comprising:

a detecting step of detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting the processor to a power saving mode , wherein said signal is detected on a bus to which the processor is connected;

an allowing step of allowing a memory controller to set the memory to a power saving mode; and

a setting step of setting the memory to the power saving mode in a case where the memory controller is allowed in said allowing step to set the memory to the power saving mode and where said signal is detected in said detecting step.

54. (New) A power saving controlling method according to claim 53, wherein the signal detected in said detecting step relates to an instruction fetch transfer for fetching the power saving mode transfer instruction from the memory for setting the processor to the power saving mode.

55. (New) A power saving controlling method according to claim 53, wherein the memory is set in said setting step to the power saving mode saving mode after an end of memory transfer in progress in a case where the memory controller is allowed in said allowing step to set the memory to the power saving mode and where the signal relating to reading the power saving mode transfer instruction from the memory for setting the processor to the power saving mode is detected in said detecting step.